UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/737,245	12/13/2000	Steven Teig	SPLX.P0012	8353

23349 7590 12/04/2002

STATTLER JOHANSEN & ADELI
P O BOX 51860
PALO ALTO, CA 94303

EXAMINER
DO, THUAN V

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/737,245	TEIG ET AL.	
	Examiner	Art Unit	
	Thuan Do	2825	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *43-64* is/are pending in the application.

4a) Of the above claim(s) *1-42,65-87* is/are withdrawn from consideration.

5)☒ Claim(s) *58-64* is/are allowed.

6)☒ Claim(s) *43-45,48,49 and 52-57* is/are rejected.

7)☒ Claim(s) *46,47,50 and 51* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 43-64 are pending in this office action. Claims 1-42 and 65-87 have been canceled.

Specifications

Figures 10A, 10B, 12A, 12B, 14A, 14B, 19A, 19B, 23A, 23B, 24A, 24B, 25A and 25B are not specified in the specification section. Correction is required.

Double Patenting

2. A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims 43-64 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 43-64 of copending Application No. 09/731,891. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

The 43-64 claims of this application are identical to the 43-64 claims of copending Application No. 09/731,891 and rejected as following:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1,2,14-23,31-36,41-45,48,49,52-57 are rejected under 35 U.S.C. 102(b) as being unpatentable over Rostoker et al., Pat. No. 5,973,376.

Regarding claim 1: Rostoker teaches a method comprising:

For an electronic design automation application (col. 6, lines 7-30 describing semiconductor device design using computer aid design CAD) , a method of placing circuit modules in an integrated circuit ("IC") layout (col. 52, lines 9-24 using cell placement in the circuit layout) , the method comprising using a diagonal line (col. 81, lines 1-9 using diagonal interconnect line) to measure a placement metric (as described by different cost calculation functions in the specification , page 4, that is matched in col. 86, lines 1-7 by using optimized functions to get a cost factor).

Regarding claim 2: Rostoker teaches a method with measure congestion (col. 1, lines 46-55 where the wire length and interconnect congestion are minimized).

Regarding claim 14: Rostoker teaches for an electronic design automation application (col. 6, lines 7-30 describing semiconductor device design using computer aid design CAD) , a method of placing circuit elements in an integrated circuit layout (col. 52, lines 9-24 using cell placement in the circuit layout), said layout using a wiring model that includes Manhattan and diagonal lines (col. 4, lines 54-60) , the method comprising using a diagonal line (col. 81, lines 1-9 using diagonal interconnect line) to measure a cost of a placement configuration (as described by different cost calculation functions in the specification, page 4, that is matched in col. 86, lines 1-7 using optimized functions to get a cost factor).

Regarding claim 15: Rostoker teaches a method with measure congestion (col. 1, lines 46-55 where the wire length and interconnect congestion are minimized).

Regarding claim 16: Rostoker teaches a method with placement cost (col. 86, lines 1-7).

Regarding claims 17,20: Rostoker teaches a method with:

a) modifying the position (col. 45, lines 35-42 where the placement is replace by a new placement);

b) measure placement cost after modification (col. 45, lines 35-42 where the shuffled placement is performed after the change in cost is evaluated).

Regarding claim 18: Rostoker teaches a method with Manhattan lines and diagonal lines (col. 4, lines 54-60).

Regarding claim 19: Rostoker teaches a method with placement cost (col. 86, lines 1-7).

Regarding claims 21,22: Rostoker teaches a method with pins of circuit module (col. 58, lines 22-34).

Regarding claim 23: Rostoker teaches a method comprising:

a) constructing a bounding box that encompasses the circuit elements of the net (Figure 93B bounded box by three side edges 4252, 4254 and 4256 containing circuit elements); and

b) using a diagonal line to measure an attribute (line) of the bounding box (col. 16, lines 42-49 using an orthogonal coordinate line system for the bounding box) .

Regarding claim 31: Rostoker teaches a method with 45 degrees (col. 81, lines 1-9).

Regarding claim 32: Rostoker teaches a method with 120 degrees (col. 17, lines 7-15).

Regarding claims 33,34: Rostoker teaches a method with pins of circuit module (col. 58, lines 22-34).

Regarding claim 35: Rostoker teaches a method comprising:

a) for each particular net, constructing a bounding box that encompasses the circuit elements of the particular net (col. 16, lines 42-49 using an orthogonal coordinate system for the bounding box net elements) ;

b) for each particular bounding box, measuring an attribute of the particular bounding box, wherein the method uses diagonal lines to measure the attributes of some of the constructed bounding boxes (col. 16, lines 42-49 using an orthogonal coordinate system for the attribute line of bounding box elements); and

c) combining said attribute measurements to obtain an estimate of interconnect-line length necessary to connect the circuit elements of the nets in the IC layout (col. 83,

lines 20-33 using various combinations of edge line attribute elements in the cell net circuit) .

Regarding claim 36: Rostoker teaches a method with adding measurements (col. 56, lines 8-16 by adding connection lengths together).

Regarding claims 41,42: Rostoker teaches a method with pins of circuit module (col. 58, lines 22-34).

Regarding claim 43: Rostoker teaches a method comprising:

constructing a connection graph that models the topology of interconnect lines for connecting the circuit elements of the net (figure 6 display a graph for interconnect wires in circuit elements),

said connection graph having edges, each edge connecting two circuit elements of the net (col. 60, lines 1-9 for connection of edges using graph) , wherein at least one of the edges is at least partially diagonal (figure 8 for diagonal connection) .

Regarding claim 44: Rostoker teaches a method with calculation of length and edges and their combinations layout (col. 83, lines 20-33 using various combinations of edge line attribute elements in the cell net circuit) .

Regarding claim 45: Rostoker teaches a method with adding measurements (col. 56, lines 8-16 by adding connection lengths together).

Regarding claim 48: Rostoker teaches a method with the combined length calculation provides an estimate of interconnect-line length needed to connect the circuit elements of the net (col. 56, lines 8-16 where the repeating process can provide the estimation the length until the total length completed).

Regarding claim 49: Rostoker teaches a method with placement cost (col. 86, lines 1-7).

Regarding claim 52: Rostoker teaches a method with 45 degrees (col. 81, lines 1-9).

Regarding claim 53: Rostoker teaches a method with 120 degrees (col. 17, lines 7-15).

Regarding claims 54,55: Rostoker teaches a method with pins of circuit module (col. 58, lines 22-34).

Regarding claim 56: Rostoker teaches a method with connection graph (figure 6) and a minimum spanning tree (col. 58, lines 60-67).

Regarding claim 57: Rostoker teaches a method with a Steiner tree (col. 59, lines 41-51).

Allowable Subject Matter

4. Claims 3,4-13,24-30,37-40,46-47,50,51 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The reason for allowance of claim 3: The prior art of record fails to teach measuring the number of nets that have circuit elements in both the sub-regions created by the diagonal cut line.

The reason for allowance of claims 4-13,24-30,37-40,51: The prior art of record fails to teach measurement of the length of at least one line that is at least partially diagonal.

The reason for allowance of claims 46-47,50: The prior art of record fails to teach calculating the distance (D).

64

Allowable Subject Matter

5. Claims 58-87 are allowed.

The reason for allowance of claims 58-64: The prior art of record fails to teach partially diagonal in combination with other features of independent claims.

The reason for allowance of claims 65-78: The prior art of record fails to teach measuring the number of nets that have circuit elements in both the sub-regions created by the diagonal cut line in combination with other features of independent claim.

The reason for allowance of claims 79-87: The prior art of record fails to teach changing the positions of the circuit modules between the sub regions to minimize the number of nets intersected by the diagonal cut line in combination with other features of independent claim.

CONTACT INFORMATION

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuan Do whose telephone number is 703-305-2362. The examiner can normally be reached on Monday-Friday 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 703-308-1323. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9318 for regular and (703) 872-9318 after final communication.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0596.

Thuan Do
Patent examiner
12/2/02